AMENDMENTS TO THE SPECIFICATION

Please replace the subtitle on page 1 as follows:

Technical Field ~~of the Invention~~

Please replace paragraph 0001 with the following amended paragraph:

0001 The present invention relates to an input and output driver and, more specifically, to an input and output driver capable of effectively reducing an input capacitance ~~Cin~~ (Cin) of a double data rate (DDR)-III ~~DDR-III~~ product.

Please replace paragraph 0002 with the following amended paragraph:

0002 Double data rate (DDR)-III standard graphic DRAM products require a channel impedance of 40Ω in which at least 30Ω tuning is supported. Furthermore, an on-die termination (ODT) circuit, which is provided ~~in a GDRAM in order~~ to match impedance between a graphic processor unit (GPU) and a graphic DRAM (GDRAM), requires impedance of about 60Ω. Furthermore, in the GDRAM, the input capacitance Cin is limited to 3pF or less to insure transmission of signal wave forms at the time of high-speed operation of 700MHz level.

Please replace paragraph 0004 with the following amended paragraph:

0004 Furthermore, increase in the capacitance due to an ODT switch transistor necessary for the ODT circuit makes it very difficult to satisfy requirements for the input capacitance Cin. ~~The more increased a~~ An increase in the memory operation frequency ~~is, the more decreased a~~ requires a decrease in the maximum allowable value of the input capacitance ~~is~~. Therefore, in order to reduce the input capacitance Cin, synthetic improvements, such as improvements ~~of~~ in design approach ~~in addition to decrease~~ and decreases in relevant processes and design rules, are required.

Please replace the title on page 2 as follows:

SUMMARY OF THE ~~INVENTION~~ DISCLOSURE

Please replace paragraph 0005 with the following amended paragraph:

0005 Therefore, ~~the present invention is contrived~~ to solve the aforementioned problems in the art, ~~and the present invention is directed to~~ an input and output driver is disclosed that is capable of effectively reducing an input capacitance Cin of a DDR-III product.

Please replace paragraph 0006 with the following amended paragraph:

0006 According to a preferred embodiment, ~~of the present invention, there is provided~~ an input and output driver is disclosed that is capable of effectively reducing an input capacitance Cin of a DDR-III product as well as satisfying ODT operation conditions requirements specified in a DDR-III product standard.

Please replace paragraph 0007 with the following amended paragraph:

0007 One ~~aspect of the present invention is to provide an~~ disclosed input and output driver ~~comprising~~ comprises: an input buffer for supplying an input data from a DQ pad to a memory cell array in a writing mode; an output driver for supplying an output data from the memory cell array to the DQ pad in a reading mode; and a DQ switch for electrically isolating the output driver from the DQ pad in the writing mode.

Please replace paragraph 0008 with the following amended paragraph:

0008 The above and other ~~objects,~~ advantages and features of the ~~present invention~~ disclosed drives will become apparent from the following description of preferred embodiments given in conjunction with accompanying drawings, ~~in which~~ where:

Please replace paragraph 0009 with the following amended paragraph:

0009 Fig. 1 is a block diagram of an input and output driver according to a ~~preferable~~ preferred ~~embodiment of the present invention~~.

Please replace paragraph 0017 with the following amended paragraph:

0017 ~~According to an aspect of the present invention, an~~ A disclosed input and output driver ~~comprising~~ comprises: an input buffer for supplying input data from a DQ pad to a memory cell array in a writing mode; an output driver for supplying output data from the memory cell array to the DQ pad in a reading mode; and a DQ switch for electrically isolating the output driver from the DQ pad in the writing mode.

Please delete paragraph 0018 as follows:

~~0018 Now, preferable embodiments of the present invention will be described with reference to accompanying drawings. However, the present invention is not limited to the preferred embodiments disclosed in the following description, but can be implemented into various changes and modifications. Thus, these embodiments according to the invention are for informing those skilled in the art of the scope of the present invention.~~

Please replace paragraph 0019 with the following amended paragraph:

0019 Fig. 1 is a block diagram of an input and output driver according to a ~~preferable~~ preferred embodiment ~~of the present invention~~.

Please replace paragraph 0020 with the following amended paragraph:

0020 Referring to Fig. 1, an input and output driver according to a preferred embodiment ~~of the present invention~~ comprises an input buffer 10, an output driver 20, and a DQ switch 30, and is connected to a DQ pad 40.

Please replace paragraph 0023 with the following amended paragraph:

0023 As shown in Fig. 1, in the writing mode, data from the DQ pad 40 is transmitted to a memory cell array (not shown) through the input buffer 10. As a result, in the writing mode, writing operation is performed through the input buffer 10 regardless of operation of the output driver 20. Therefore, in the writing mode, the input and output driver according to a preferred embodiment ~~of the present invention~~ electrically isolates the output driver 20 from the DQ pad 40 using the DQ switch 30. As a result, it is possible to reduce increment in capacitance due to the output driver 20. On the other hand, in the reading mode, data DATAO sensed from the memory cell array is output to the DQ pad 40 through the

output driver 20. Therefore, in the reading mode, the DQ switch 30 is turned-on to electrically connect the output driver 20 to the DQ pad 40.

Please replace paragraph 0024 with the following amended paragraph:

0024 The DQ switch 30 comprises ~~an~~ a low voltage threshold LVT (LOW VT) NMOS transistor LNM or an LVT PMOS transistor LPM, as shown in Fig. 2A. For example, a threshold voltage VT of the LVT NMOS transistor LNM or the LVT PMOS transistor LPM is preferably 0.15V or less. In addition, a gate voltage VG of the LVT NMOS transistor LNM is preferably a pumping voltage VPP (3.5V or more) instead of a power source voltage VDD (1.8V). The pumping voltage VPP is generally twice the power source voltage. On the other hand, a gate voltage of the LVT PMOS transistor LPM is preferably a negative pumping voltage '–VPP' or a ground voltage VSS.

Please replace paragraph 0030 with the following amended paragraph:

0030 Generally, as shown in Fig. 6, in order to match impedance between a GPU 200 and a GDRAM 100, an ODT circuit 70 is provided in a GDRAM 100. The ODT circuit 70 requires an impedance of 60Ω. In the input and output driver according to the preferable embodiment of the present invention, the ODT circuit 70 is provided between a voltage source and a node N which is connected to the DQ switch 30 and the DQ pad 40. Specifically, as shown in Fig. 7, the ODT circuit 70 is connected between the node N and the voltage source for supplying the power source voltage VDD. The ODT circuit 70 is comprised of an ODT switch ODTS and an ODT resistor ODTR. The ODT switch ODTS is controlled by control signals GPUCA of the GPU 200. Furthermore, as shown in Fig. 8, the input and output driver further comprises ~~an~~ electrostatic discharge protection ESD circuit 80 and a charged device model CDM 90 in addition to the ODT circuit 70. The ESD circuit 80 comprised of ESD transistors ESDU and ESDD connected in serial is provided between the DQ pad 40 and the CDM circuit 90. The CDM circuit 90 comprised of a CDM transistor CDMT and a CDM resistor CDMR is provided between the input buffer 10 and the ESD circuit 80.

Please replace paragraph 0033 with the following amended paragraph:

0033 ~~In the aforementioned description, although spirit of the present invention has been described in detail using the preferable embodiments, the preferable embodiments will be provided for more complete explanation of the present invention to those skilled in the art. Therefore, it is noted that the present invention~~ This disclosure is not limited to the embodiments disclosed above and in the drawings. ~~However~~ Further, it ~~is~~ will be understood that various changes and modifications may be made to the embodiments by those who skilled in the art without departing from the spirit of ~~the present invention~~ this disclosure or the appended claims.

Please replace paragraph 0034 with the following amended paragraph:

0034 As described above, ~~according to the present invention,~~ it is possible to reduce the total input capacitance Cin by electrically isolate the output driver from the DQ pad using the DQ switch in the writing mode to reduce the capacitance due to the output driver.

Please replace paragraph 0035 with the following amended paragraph:

0035 Furthermore, it is possible to effectively reduce the input capacitance Cin as well as to satisfy an ODT operation condition of the DDR-III standard by providing the ODT circuit and the DQ switch to the input and output driver ~~according to the present invention~~.